patent teaches the limitation "wherein said testing and storing are performed outside of a production facility of said die," as recited in claim 1, or "in a field," as recited in claim 64. Nor do claim 1 or claim 56 of the '072 patent claims teach that "said testing and storing are performed when said die is part of a processing system." Furthermore, the Applicant notes that during subsequent prosecution the claims of the present application may be amended to make this rejection unnecessary. Additionally, the Applicant notes that the claims can be fully considered now without this issue being immediately addressed. As such, the Applicant respectfully requests that the double patenting rejection be held in abeyance until allowable subject matter is indicated, or that the rejection be withdrawn.

Claims 1 and 64-65 stand rejected under 35 U.S.C. § 101 and 35 U.S.C. § 112, first paragraph, as not supported by either a specific and substantial asserted utility or a well established utility. The Office Action states that the limitation of "wherein said storing replaces any previously stored address or partial address" is not supported by the specification or drawings. Applicant directs attention to paragraph [0051] of the specification, which states: "Once the chips have been repaired, they may undergo a repeat of the previous test. Alternatively, they and the chips that passed the previous test may be subjected to a different test. In such cases, the address and fail-flag value may be cleared from the repaired chips' address registers 32 before testing continues, and the testing process proceeds as described above." When the testing proceeds, new address and flag values are stored. Paragraph [0041]. Accordingly, the limitation quoted in the Office Action is fully supported and Applicant respectfully requests that the rejection of these claims be withdrawn and the claims allowed.

Claim 66-67 stand objected to for informalities. The Office Action requests that the word "cell" in line 2 of each of claims 66 and 67 should be changed to "cells." For example, claim 66 reads "wherein said storing in a register at least a partial address of

any defective memory cell comprises storing a column address of the defective memory cell." It should be noted, however, that the claim limitation refers to "any defective memory cell," which is grammatically a singular noun, and the limitation refers to an address of such a cell. Applicant respectfully requests that the objection to these claims be withdrawn and the claims allowed.

Claims 1-6 and 64-65 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Brauch et al. (US 6,550,023). This rejection is respectfully traversed. In order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. §2142. Brauch et al., even when considered in combination with the assertion of obviousness in the Office Action, does not teach or suggest all limitations of independent claims 1, 64, or 65.

Claim 1 recites a method of testing a memory die comprising, *inter alia,* a method of testing a memory die, comprising "testing said memory die; and storing in said memory die at least a partial address of any defective memory cell found during said testing, wherein said storing replaces any previously stored address or partial address, said at least a partial address corresponding to a memory cell having failed said testing, wherein said testing and storing are performed outside of a production facility of said die." (emphasis added). Claims 64-65 recite similar limitations. Applicant respectfully submits that Brauch et al. does not disclose, teach, or suggest these limitations.

To the contrary, Brauch et al. teaches that "the comparison mismatch information is stored in a bitmap storage 18 located on-chip for later retrieval by external hardware. The accumulated mismatch pairs at the end of the test comprise a complete bitmap of the precise location of failed cells in memory 4 that were detected by the particular memory test executed by BIST functional block 6." Col. 3, ln. 42-48

(emphasis added). Applicants respectfully submit that Brauch et al. does not disclose, teach, or suggest "storing in said memory die at least a partial address of any defective memory cell found during said testing, wherein said storing replaces any previously stored address or partial address," as recited in claims 1, 64, and 65. Nor does the Office Action assert that Brauch et al. teaches or suggests this limitation. Although the Office Action asserts (at p. 4) that "testing and storing would have been performed outside of a production/manufacturing facility of a die" would be obvious to one skilled in the art, this would not cure the above-described deficiencies. Thus, the assertion does not remedy the deficiency of Brauch et al.

Since Brauch et al. does not teach or suggest all of the limitations of claims 1, 64, and 65, claims 1, 64, and 65 are not obvious over Brauch et al. Claims 2-5 depend, respectively, from claim 1, and are patentable at least for the reasons mentioned above, and on their own merits. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 1-6 and 64-65 be withdrawn and the claims allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By _____

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